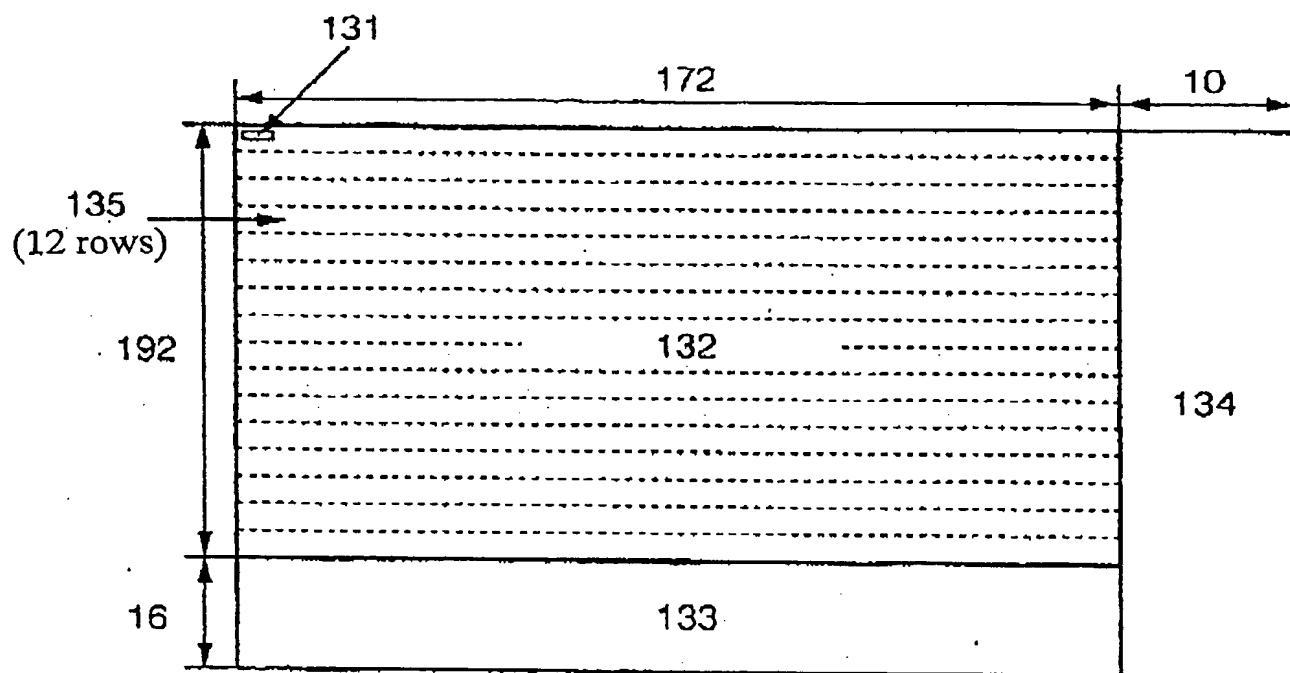


FIG. 1 prior art



T07E80" 0E24660

FIG. 2

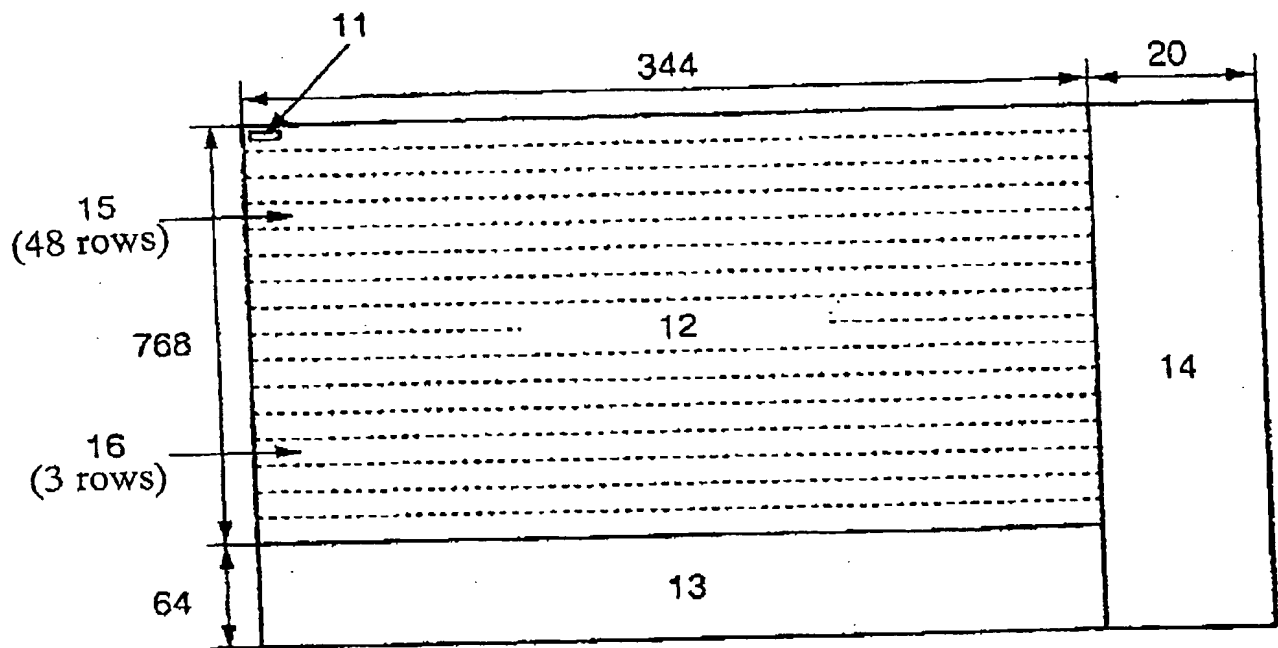
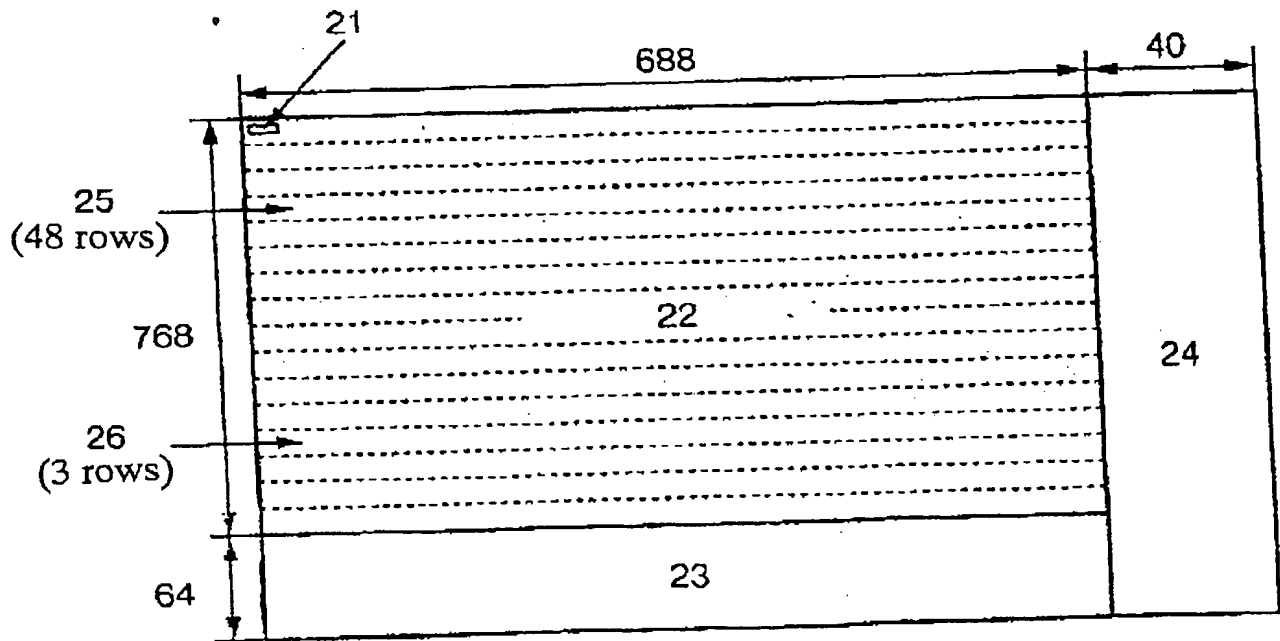


FIG. 2 OF 2

FIG. 3



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FIG. 4

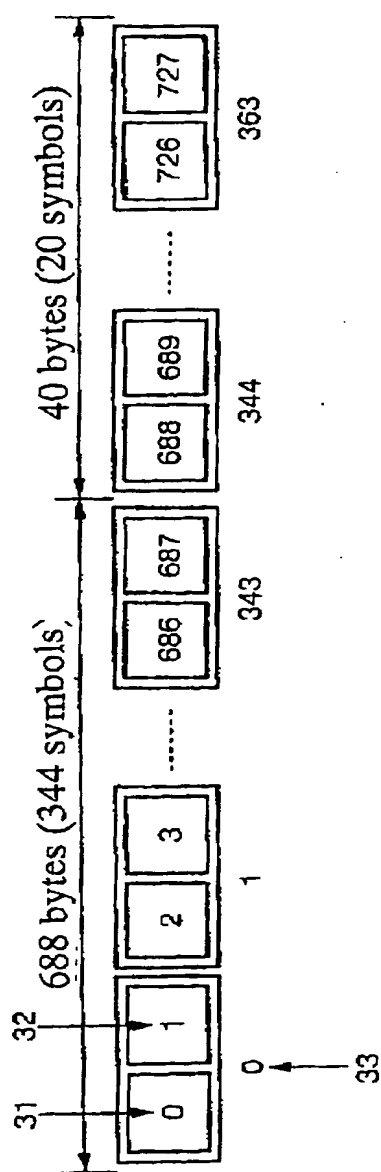
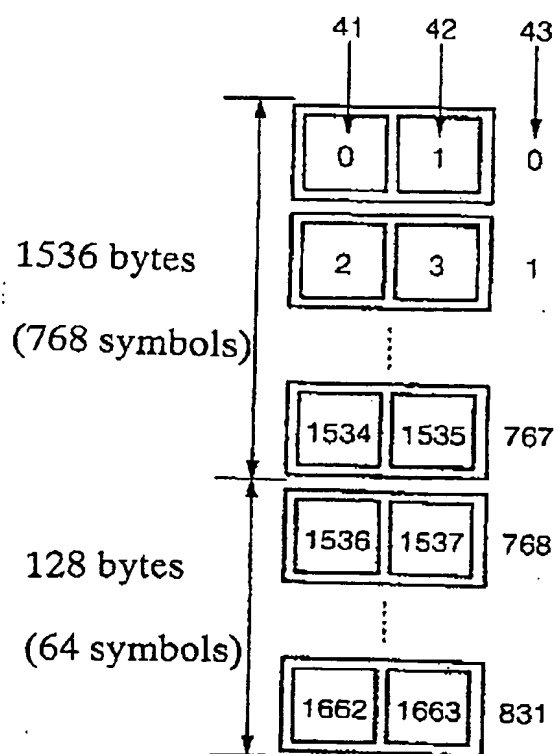


FIG. 5



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FIG. 6

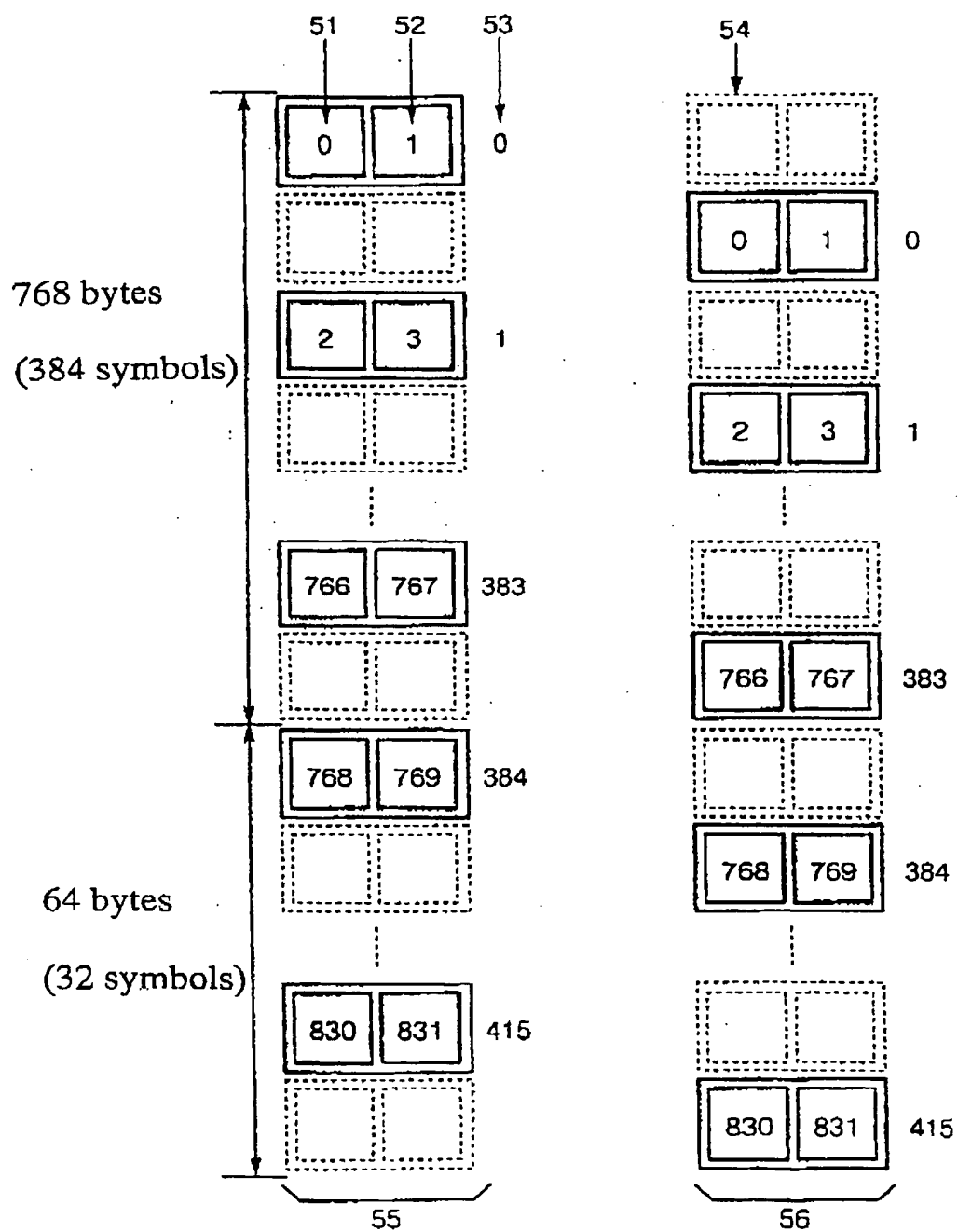
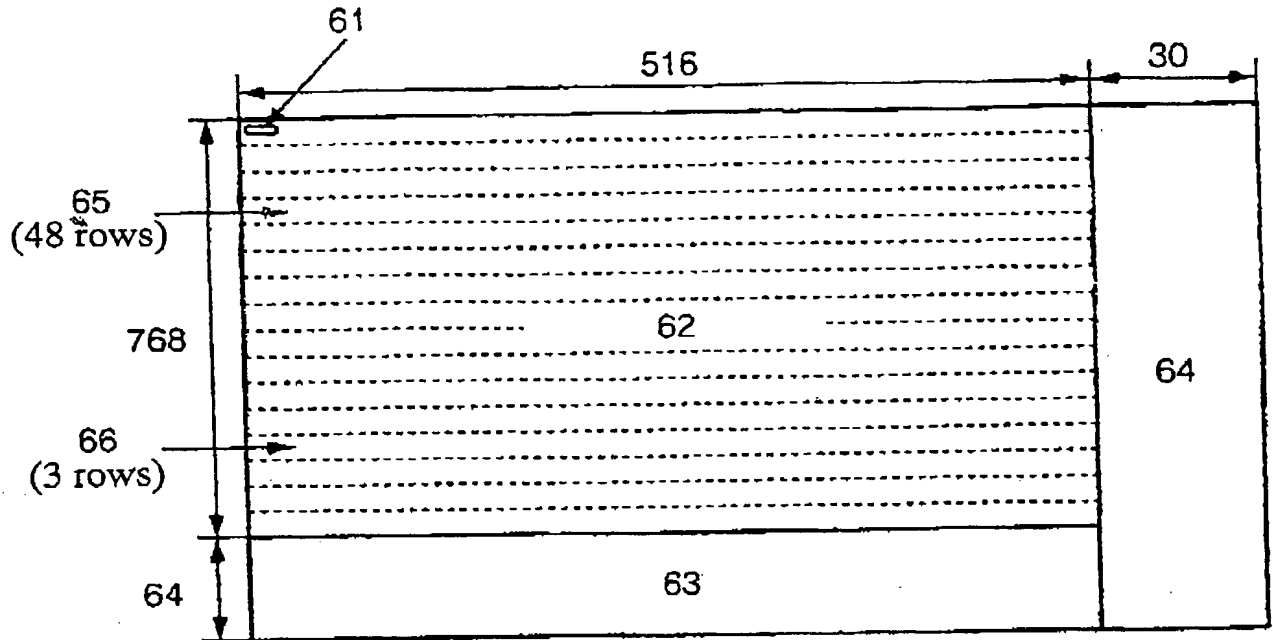


FIG. 7



TOTAL OF 24660

FIG. 8

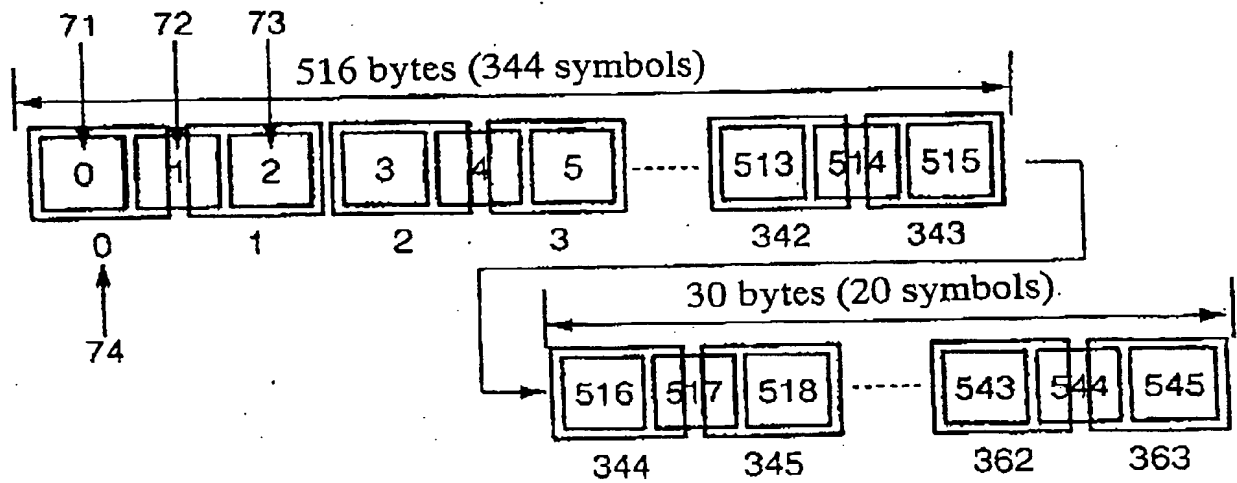




FIG. 9

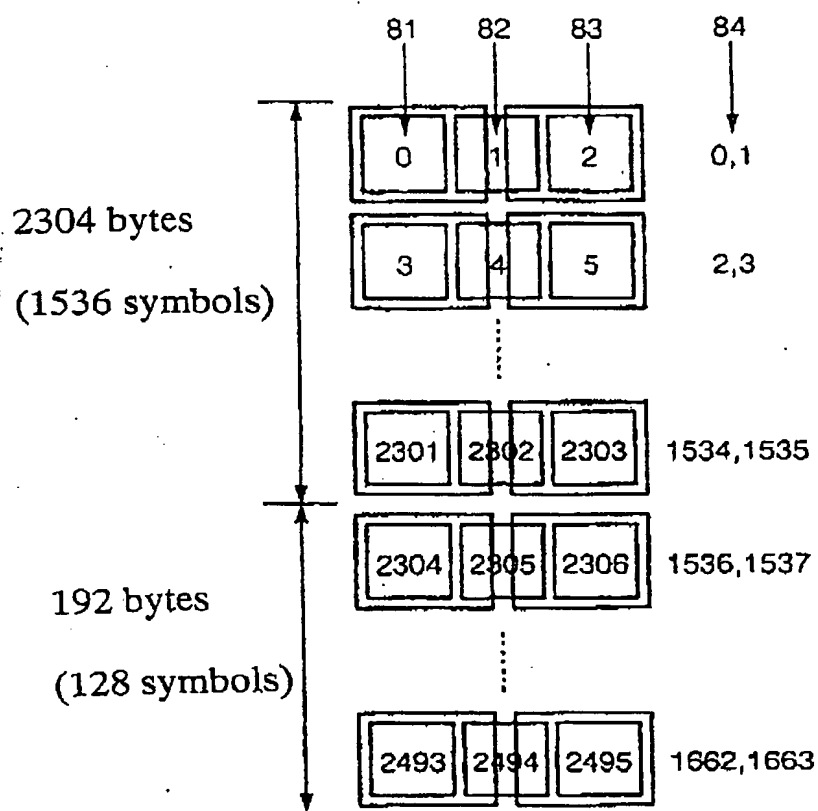


FIG. 10

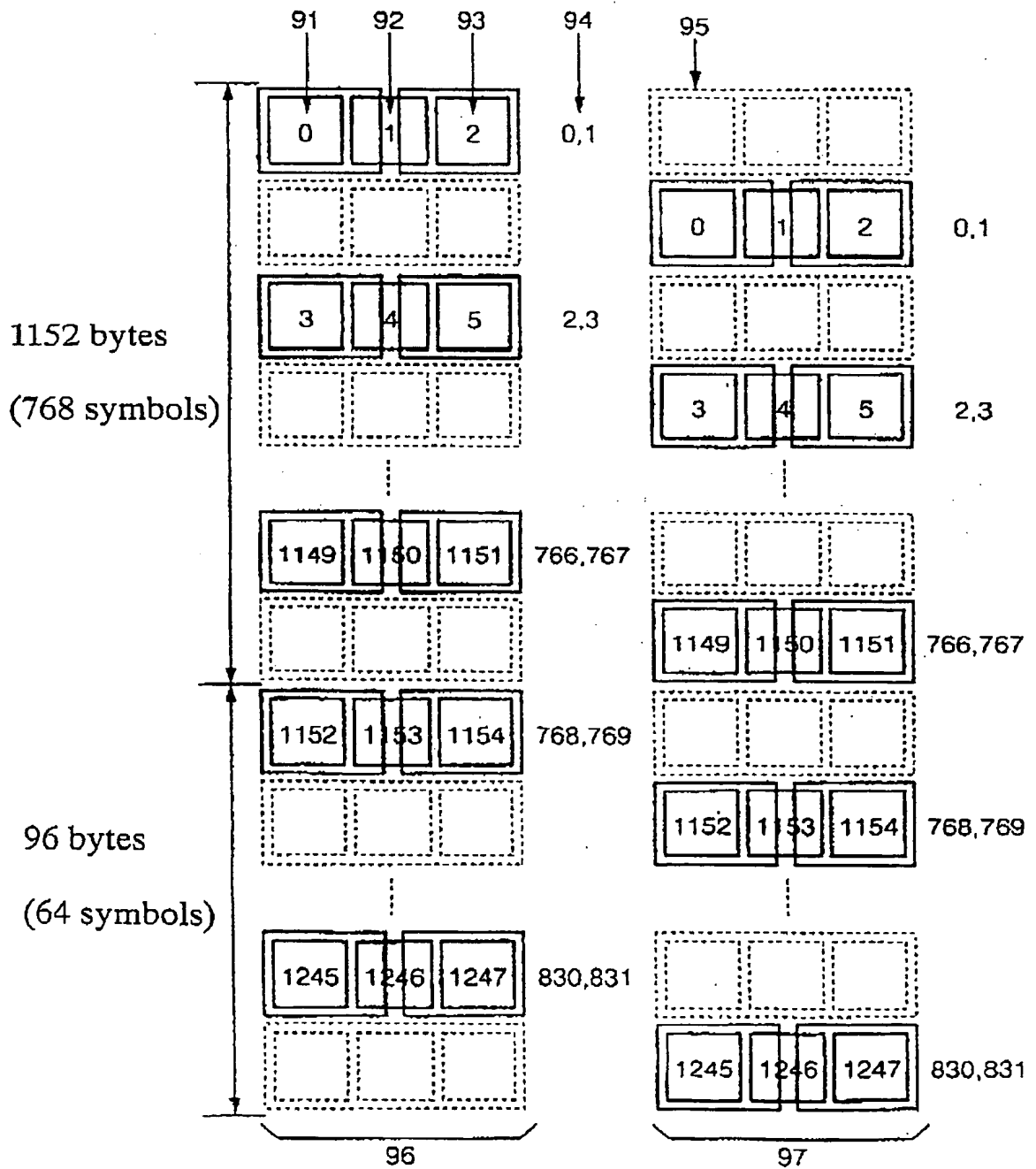
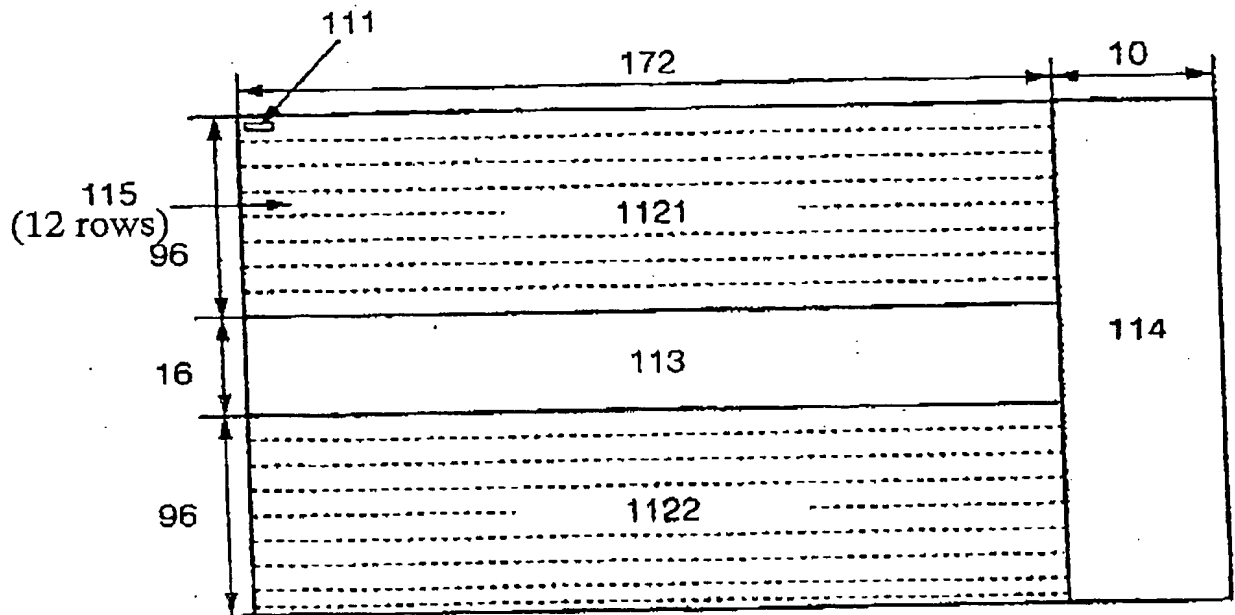


Diagram illustrating a memory array layout. The array is organized into rows and columns. The top row is labeled 101. The first column is labeled 103 (12 rows) and 104 (1 row). The second column is labeled 102. The third column is labeled 105. The total width of the array is labeled 172. The total height of the array is labeled 10.

FIG. 12



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FIG. 13

